In the specification:

Please replace the BRIEF DESCRIPTION OF DRAWINGS section beginning at page 5, line 11 and ending at page 6, line 22 with the following BRIEF DESCRIPTION OF DRAWINGS section:

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a top view of first and second active areas defining memory cell footprints on a semiconductor substrate in accordance with the present invention.

Fig. 2 is a side sectional view of the memory cell footprint illustrated in Fig. 1, taken along lines 2-2, with isolation regions bordering active areas.

Fig. 3 is a top view of a memory cell footprint as in Fig. 1, with an overlay of a mask for doping substrate regions.

Fig. 4 is a side sectional view along lines 4-4 in Fig. 3.

Fig. 5 is a top view of a memory cell footprint as in Fig. 3, with a first polysilicon layer etched to a rectangular pattern.

Fig. 6 is a side section view along lines 6-6 in Fig. 5.

Fig. 7 is a top view of a memory cell footprint as in Fig. 5, with a tunnel oxide layer etched to a rectangular pattern and an overlying second polysilicon layer overlying the oxide layer removed except for a poly spacer region appearing as a rectangle.

Fig. 8 is a side sectional view along lines 8-8 in Fig. 7.

Fig. 9 is a top view of a memory cell footprint as in Fig. 7, with a third polysilicon layer overlying other layers.

Fig. 10 is a side sectional view along lines 10-10 in Fig. 9, showing source and drain implants and a TEOS layer, all applied before the third polysilicon layer of Fig. 9.

Fig. 11 is a side sectional view showing the structure of Fig. 10 with a photomask over the central raised third polysilicon layer.

Fig. 12 is a top view of a memory cell footprint as in Fig. 9, with a new third polysilicon boundary formed by etching to the substrate.

Fig. 13 is a side sectional view along lines 13-13 in Fig. 12 with additional ILD and contact mask layers over the entire structure.

Fig. 14 is a side sectional detail of a cut through the layers shown in Fig. 13.

Fig. 15 is a top view of a memory cell footprint as in Fig. 12, with contact positions shown.

Fig. 16 is a side sectional detail as in Fig. 14, with the cut being filled and capped.

Fig. 17 is a side sectional view along lines 16-16 in Fig. 16.

Please replace the paragraph beginning at page 8, line 10 and ending at page 8, line 23 with the following paragraph:

In Figs. 5 and 6, those portions of the gate oxide layer extending beyond the footprint edges 52, 56, 54, 58 of the first etched poly layer 51 are removed. Upon removal, there is a single ion implantation of electrodes including a first electrode implant region 71 and a second electrode implant region 73, with the first electrode implant region being a future source electrode and the second electrode implant region 73 being a future drain electrode implant within the implant mask region 41. Note that the implant

regions are barely below the surface of the substrate. The main floating body 51 acts as alignment mask for the first and second electrode implant regions 71 and 73 so that these electrodes are essentially self aligned with the left and right edges of the rectangular main floating body 51.

Please replace the section beginning at page 9, line 3 and ending at page 10, line 34 with the following section:

In ~~Fig. 8~~ Figs. 7 and 8 and as described above, the gate oxide layer 53 is seen to be above substrate 31 and above implant mask region 41. The first polysilicon layer 51, etched to a rectangular main floating body, is seen to be above the gate oxide layer. Now, the thin tunnel oxide layer 61 is grown over the main floating body, extending over the substrate on both sides. The thin oxide layer has a vertical portion 63 rising along a vertical wall of the first polysilicon layer and then having a top mesa portion 65, sometimes called poly oxide. The thickness of the thin oxide layer is in the range of 30-70 Angstroms.

In Fig. 8, conductive polysilicon spacers 67 and 69 are seen to resemble nitride spacers of the prior art and be insulated from the first polysilicon layer 51 by the vertical portion 63 of the tunnel oxide. The spacers are also insulated from the substrate by the tunnel oxide layer 61. It will be seen that both the main floating body 51, as well as the poly spacer 69 both reside above the subsurface ion implantation region [55] 45. The ion implantation region can supply charge, i.e. electrons, to both the main floating body 51 as well as the poly spacer 69 through a vertical portion 63 of the tunnel oxide. In other words, electrons migrating through the tunnel oxide have two paths to reach a floating member, with one path being into the main floating body 51 and the other path being into the poly spacer 69. This is thought

to enhance the probability of electron capture into a floating body.

With reference to Fig. 9, a third poly layer 77 is deposited over the top of the structure seen in Fig. 8. The function of the third poly layer will be to electrically connect the first and second layers. In Fig. 10, the third ~~capping dielectric~~ poly layer 77 is seen to itself be capped by a dielectric layer 75 which may be a TEOS layer which follows the contours of the structure below so that the mesa feature described above is preserved. In Fig. 11, the mesa feature has been simplified by a single body 83 which includes all of the elements seen in Fig. 10, both above the upper surface of the substrate and below. A photomask 81 is applied over the mesa feature, well within the isolation regions 28 and 29. The photomask 81 allows removal of all layers to the outside of the mask, stopping at the substrate. Once all layers outside the mesa structure are removed, the mask itself is removed.

Considering Figs. 12, 13, and 14, an interlayer dielectric (ILD) region 85 is applied directly over the substrate, over the implant mask region 41 and over the mesa feature. A photoresist contact mask 87 is applied above the dielectric layer 85. A cell contact 89 is located longitudinally outside of the active area over a portion of the isolation region. In Fig. 13 it may be seen that a hole 82 is patterned in the photoresist layer 87, with the hole extending into the mesa feature, with the hole near but not contacting poly spacer 69. The hole extends through a portion of the rectangular main floating body 51. In Fig. 14 the hole may be seen to extend through the floating body 51, the poly oxide 65, the third poly layer 77, the ILD layer 85, and the contact photomask layer 87.

In Fig. 15, the hole 82 is seen to be filled with a metal filler 91, preferably a tungsten plug which may be sputtered into the hole, covered by contact 93. Poly spacer

69 is seen to make contact with third poly layer 77. In turn, the metal plug 91 connects the third layer 77 with the main floating body 51 so that the main floating body and the poly spacer are at the same electrical potential, a very important connection.

Please replace the paragraph beginning at page 11, line 14 and ending at page 11, line 18 with the following paragraph:

Returning to Fig. 16, the dimension L_s indicates the relative length of the source, while the dimension L_D, seen above the implant mask region 41, indicates the relative length of the drain. L_D is much greater than L_s. This leads to C_{gs} being much smaller than C_{gd}.

Conclusion

In response to the Office action mailed May 17, 2004 Applicant is correcting the placement of reference numerals in the text to correspond to these numerals in the drawings. Applicant thanks the Examiner for pointing out the omissions.

Applicant asserts that the amendments made to the specification do not incorporate any new matter. Applicant respectfully submits that the application is now in condition for allowance. Accordingly, a Notice of Allowance is respectfully requested.

CERTIFICATE OF MAILING

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Signed: Sally Azevedo
Typed Name: Sally Azevedo

Date: July 16, 2004

Respectfully submitted,

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